

- 1 What is claimed is:
- 2 1. A flip-chip package comprising:
- 3 a substrate having a top surface, a bottom surface and an opening passing through the
- 4 top surface and the bottom surface;
- 5 a dummy die disposed on the bottom surface of the substrate corresponding to the
- 6 opening, wherein the dummy die has a surface with a redistribution layer (RDL)
- 7 electrically connected with the substrate and
- 8 a chip flip-chip mounted on the surface of the dummy die inside the opening, and
- 9 electrically connected with the redistribution layer of the dummy die.
- 10 2. The flip-chip package of claim 1, further comprising a packaging body formed at the
- 11 opening of the substrate.
- 12 3. The flip-chip package of claim 1, wherein the substrate is a printed circuit board.
- 13 4. The flip-chip package of claim 1, wherein the dummy die is larger than the chip in
- 14 size.
- 15 5. The flip-chip package of claim 1, wherein the redistribution layer of the dummy die
- 16 includes a plurality of flip-chip pads and a plurality of connecting pads arraying at the
- 17 perimeters of the dummy die.
- 18 6. The flip-chip package of claim 5, wherein the flip-chip pads have a pitch smaller than
- 19 that of the connecting pads.
- 20 7. The flip-chip package of claim 6, wherein the pitch of the flip-chip pads is smaller than
- 21 150 μm .
- 22 8. The flip-chip package of claim 5, further comprising a plurality of bonding wires
- 23 connecting the connecting pads of the redistribution layer to the substrate.
- 24 9. The flip-chip package of claim 5, further comprising a plurality of bumps bonding the
- 25 connecting pads of the redistribution layer to the substrate.
- 26 10. The flip-chip package of claim 1, further comprising a plurality of solder balls formed
- 27 on the bottom surface of the substrate.

- 1 11. The flip-chip package of claim 10, wherein the substrate has a plurality of connection
2 pads on the top surface electrically connected with the solder balls.
- 3 12. The flip-chip package of claim 11, further comprising a stack semiconductor package
4 is disposed on the top surface of the substrate, the stack semiconductor package
5 includes a plurality of outer terminals connecting with the connection pads.
- 6 13. The flip-chip package of claim 1, wherein the substrate has a stair around the
7 opening.
- 8 14. The flip-chip package of claim 1, wherein the dummy die has an exposed surface
9 corresponding to the surface with the redistribution layer, a thermal-conducting layer
10 is formed on the exposed surface.
- 11 15. The flip-chip package of claim 14, wherein the thermal-conducting layer is a metal
12 layer.
- 13 16. A chip carrier for flip-chip package comprising:
14 a substrate having an top surface, an bottom surface and an opening passing through
15 the top surface and the bottom surface; and
16 a dummy die disposed on the bottom surface of the substrate corresponding to the
17 opening, wherein the dummy die has a surface with a redistribution layer (RDL)
18 electrically connected with the substrate.
- 19 17. The chip carrier for flip-chip package of claim 16, wherein the substrate is a printed
20 circuit board.
- 21 18. The chip carrier for flip-chip package of claim 16, wherein the substrate has a stair
22 around the opening.
- 23 19. The chip carrier for flip-chip package of claim 16, wherein the redistribution layer of
24 the dummy die includes a plurality of flip-chip pads and a plurality of connecting
25 pads, the connecting pads are arrayed at the perimeters of the dummy die.
- 26 20. The chip carrier for flip-chip package of claim 19, wherein the flip-chip pads have a
27 pitch smaller than that of the connecting pads.

- 1 21. The chip carrier for flip-chip package of claim 19, wherein the pitch of the flip-chip
2 pads is smaller than 150 μm .
- 3 22. The chip carrier for flip-chip package of claim 19, further comprising a plurality of
4 bumps bonding the connecting pads of the redistribution layer to the substrate.
- 5 23. The chip carrier for flip-chip package of claim 16, wherein the dummy die has an
6 exposed surface corresponding to the surface with the redistribution layer, a
7 thermal-conducting layer is formed on the exposed surface.
- 8 24. The chip carrier for flip-chip package of claim 23, wherein the thermal-conducting
9 layer is a metal layer.
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